AMENDMENTS TO THE SPECIFICATION

Please delete the section entitled "SUMMARY" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

The present invention provides a branch prediction method and apparatus that makes efficient use of chip real estate, but also provides accurate branching early in the pipeline to reduce branch penalty. Accordingly, in attainment of the aforementioned object, it is a feature of the present invention to provide a pipelined microprocessor. The microprocessor includes an instruction cache that is indexed by a fetch address. The instruction cache caches instructions and provides the instructions to an instruction buffer for storage therein. The instructions comprise variable byte-length instructions. The microprocessor also includes a branch target address cache, coupled to the instruction buffer and indexed by the fetch address, which caches branch target addresses of previously executed branch instructions. The instruction buffer includes an indicator associated with each byte of each of the instructions stored in the instruction buffer. The indicator has a true value if the branch target address cache predicts that the byte is an opcode byte of one of the instructions and that the instruction is one of the previously executed branch instructions and the microprocessor has speculatively branched to one of the branch target addresses cached for the previously executed branch instruction.

In another aspect, it is a feature of the present invention to provide a method of speculatively branching in a pipelined microprocessor. The method includes a branch target address cache (BTAC) caching a plurality of branch target addresses of previously executed branch instructions and a bit associated with each of the branch instructions. The bit is true only if the associated branch instruction spans more than one instruction cache line. The microprocessor processes variable byte-length instructions. The method also includes accessing the BTAC with a fetch address of an instruction cache after the caching. The method also includes determining whether the fetch address hits in the BTAC in response to the accessing. The method also includes branching the microprocessor to one of the plurality of branch target addresses selected by the fetch

address if the fetch address hits in the BTAC, whether or not a branch instruction is cached in a line of the instruction cache indexed by the fetch address. The method also includes storing in an instruction buffer instructions provided by the instruction cache selected by the fetch address, and storing a discrete indication for each byte of each the instruction. The discrete indication is true if the BTAC predicts the byte is an opcode byte of the instruction and the branching the microprocessor to one of the plurality of branch target addresses was performed for the instruction.

An advantage of the present invention is that it does not require indexing of the BTAC by an instruction pointer prior to the branch instruction being predicted according to a previous method, thereby avoiding the negative impact upon prediction accuracy of the previous method.

A further advantage of the present invention is that it enables an early speculative branch without the potential branch instruction being decoded by instruction pre-decode logic to determine whether a line in the instruction cache actually contains a branch instruction.

Other features and advantages of the present invention will become apparent upon study of the remaining portions of the specification and drawings.